IN THE CLAIMS

Please amend the claims as follows:

Claim 1-12 (Canceled).

Claim 13 (Currently Amended): A data storage medium comprising:

a semiconductor ~~element~~ memory device having a first memory ~~area~~ cell array, a second memory ~~area~~ cell array, ~~first wiring for controlling data write erase operations of the first memory area,~~ a first terminal ~~for controlling the first wiring~~ connected to the first memory cell array, ~~second wiring for controlling a data write operation of the second memory area,~~ and a second terminal ~~for controlling the second wiring~~ connected to the second memory cell array;

a first wiring, connected to the first terminal, for controlling data write and erase operations of the first memory cell array;

a second wiring, connected to the second terminal, for controlling a data write operation of the second memory cell array;

an external terminal connected to the second terminal and electrically separated from the first terminal;

a support material which supports the semiconductor ~~element~~ memory device and the external terminal so that the semiconductor ~~element~~ memory device is covered with the support material and the external terminal is exposed from the support material; and

certification data that is unique to the semiconductor ~~element~~ memory device, stored in the first memory ~~area~~ cell array.

14. (Previously Presented): The data storage medium of claim 13, further comprising:

a circuit which controls a conducting state arranged between the first terminal and the first wiring.

Claim 15 (Currently Amended): The data storage medium of claim 13, further comprising:

a transistor arranged between the first memory ~~area~~ cell array and the first wiring, a gate electrode of the transistor being connected to the first terminal.

Claim 16 (Currently Amended): A data storage medium comprising:

a wiring board having first and second faces;

a semiconductor ~~element~~ memory device mounted on the first face of the wiring board, having a first memory ~~area~~ cell array, a second memory ~~area~~ cell array, ~~first wiring for controlling data write erase operations of the first memory area,~~ a first terminal ~~for controlling the first wiring~~ connected to the first memory cell array, ~~second wiring for controlling a data write operation of the second memory area,~~ and a second terminal ~~for controlling the second wiring~~ connected to the second memory cell array;

a first wiring, connected to the first terminal, for controlling data write and erase operations of the first memory cell array;

a second wiring, connected to the second terminal, for controlling a data write operation of the second memory cell array;

an external terminal arranged on the second face of wiring board, connected to the second terminal, and electrically separated from the first terminal;

a resin seal for covering the first face of the wiring board and the semiconductor ~~element~~ memory device; and

certification data that is unique to the semiconductor ~~element~~ memory device, stored in the first memory ~~area~~ cell array.

Claim 17 (Currently Amended): The data storage medium of claim 16, further comprising:

a module which integrates the semiconductor ~~element~~ memory device, external terminal, and resin seal into one; and

a card-type support which supports the module.

Claim 18-30 (Canceled).

Claim 31 (Currently Amended): The data storage medium according to claim 13, wherein

the first memory ~~area~~ cell array is read-only and stores first certification data that is unique to the data storage medium and the second memory ~~area~~ cell array stores data and second certification data supplied from the outside; and

the data storage medium further comprises:

an identity circuit which determines whether or not the first and second certification data are identical with each other, and the identity circuit including a generator which generates binary data and inverted binary data from the first certification data, and an adder which adds the inverted binary data of the first certification data to binary data corresponding to the second certification data; and

a switch circuit which provides the data stored in the second memory ~~area~~ cell array to the outside only when the identity circuit determines that the first and second certification data are identical with each other, and the switch circuit including a circuit which connects

the second memory ~~area~~ cell array to an output terminal only when a sum provided by the adder includes all 1s.

Claim 32 (Currently Amended): The data storage medium of claim 31, wherein the first memory ~~area~~ cell array stores binary data and inverted binary data both corresponding to the first certification data.

Claim 33 (Currently Amended): The data storage medium of claim 32, further comprising:

a tester which checks to see if the first certification data was altered; and

another switch circuit which provides the data stored in the first memory ~~area~~ cell array to the outside only when the tester determines that the first certification data was not altered.

Claim 34 (Currently Amended): The data storage medium of claim 31, wherein the first and the second memory ~~areas~~ cell arrays are reserved in a NAND-type flash memory.

Claim 35 (Currently Amended): The data storage medium of claim 13, wherein

the first memory ~~area~~ cell array is read-only and stores first certification data that is unique to the data storage medium, and stores binary data and inverted binary data both corresponding to the first certification data, and the second memory ~~area~~ cell array stores data and second certification data supplied from the outside; and

the data storage medium further comprises:

an identity circuit which determines whether or not the first and second certification data are identical with each other;

a switch circuit which provides the data stored in the second memory ~~area~~ cell array to the outside only when the identity circuit determines that the first and second certification data are identical with each other;

a tester which checks to see if the first certification data was altered and the tester including a reader which reads the binary data and inverted binary data both corresponding to the first certification data from the first memory ~~area~~ cell array and an adder which adds the read binary data and inverted binary data to each other; and

another switch circuit which provides the data stored in the first memory ~~area~~ cell array to the outside only when the tester determines that the first certification data is not altered, and the another switch circuit including a circuit which connects the first memory ~~area~~ cell array to an output terminal only when a sum provided by the adder includes all 1s.

Claim 36 (Currently Amended): The data storage medium of claim 13, wherein

the first memory ~~area~~ cell array is read-only and stores first certification data that is unique to the data storage medium, and the second memory ~~area~~ cell array stores data and second certification data supplied from the outside; and

the data storage medium further comprises:

an encoder which encodes the first certification data into third certification data;

a specific memory area defined in the second memory ~~area~~ cell array according to the first certification data, to store the third certification data;

an identity circuit which determines whether or not the second and third certification data are identical with each other; and the identity circuit including a generator which generates binary ~~data~~ data; and

a switch circuit which provides the data stored in the second memory ~~area~~ cell array to the outside only when the identity circuit determines that the second and third certification data are identical with each other.

Claim 37 (Currently Amended): The data storage medium of claim 36, wherein the first and second memory ~~areas~~ cell arrays are reserved in a NAND-type flash memory.

Claim 38 (Previously Presented): The data storage medium of claim 36, wherein the identity circuit comprises:

a generator which generates inverted binary data from binary data corresponding to the third certification data; and

an adder which adds the inverted binary data of the third certification data to binary data corresponding to the second certification data, and to an output terminal only when a sum provided by the adder includes all 1s.

Claim 39 (Previously Presented): The data storage medium of claim 36, wherein the specific memory area stores binary data both corresponding to the third certification data.

Claim 40 (Previously Presented): The data storage medium of claim 36, further comprising:

a tester which tests to see if the third certification data was altered; and

another switch circuit which provides the third certification data to the outside only when the tester determines that the third certification data was not altered.

Claim 41 (Previously Presented): The data storage medium of claim 40, wherein the tester comprises:

a reader which reads the binary data and inverted binary data both corresponding to the third certification data from the specific memory area; and

an adder which adds the read binary data and inverted binary data to each other, and wherein the switch circuit comprises:

a circuit which connects the specific memory area to an output terminal only when a sum provided by adder includes all 1s.

Claim 42 (Currently Amended): The data storage medium of claim 16, wherein

the first memory ~~area~~ cell array is read-only and stores first certification data that is unique to the data storage medium, and the second memory ~~area~~ cell array stores data and second certification data supplied from the outside; and

the data storage medium further comprises:

an identity circuit which determines whether or not the first and second certification data are identical with each other, and the identity circuit including a generator which generates binary data and inverted binary data from the first certification data, and an adder which adds the inverted binary data of the first certification data to binary data corresponding to the second certification data; and

a switch circuit which provides the data stored in the second memory ~~area~~ cell array to the outside only when the identity circuit determines that the first and second certification data are identical with each other, and the switch circuit including a circuit which connects the second memory ~~area~~ cell array to an output terminal only when a sum provided by the adder includes all 1s.

Claim 43 (Currently Amended): The data storage medium of claim 42, wherein the first memory ~~area~~ cell array stores binary data and inverted binary data both corresponding to the first certification data.

Claim 44 (Currently amended): The data storage medium of claim 43, further comprising:

a tester which checks to see if the first certification data was altered; and

another switch circuit which provides the data stored in the first memory ~~area~~ cell array to the outside only when the tester determines that the first certification data was not altered.

Claim 45 (Currently Amended): The data storage medium of claim 42, wherein the first and the second memory ~~areas~~ cell arrays are reserved in a NAND-type flash memory.

Claim 46 (Currently Amended): The data storage medium of claim 16, wherein

the first memory ~~area~~ cell array is read-only and stores first certification data that is unique to the data storage medium, and stores binary data and inverted binary data both corresponding to the first certification data, and the second memory ~~area~~ cell array stores data and second certification data supplied from the outside; and

the data storage medium further comprises:

an identity circuit which determines whether or not the first and second certification data are identical with each other;

a switch circuit which provides the data stored in the second memory ~~area~~ cell array to the outside only when the identity circuit determines that the first and second certification data are identical with each other;

a tester which checks to see if the first certification data was altered, and the tester including a reader which reads the binary data and inverted binary data both corresponding to the first certification data from the first memory ~~area~~ cell array and an adder which adds the read binary data and inverted binary data to each other; and

another switch circuit which provides the data stored in the first memory ~~area~~ cell array to the outside only when the tester determines that the first certification data is not altered, and the another switch circuit including a circuit which connects the first memory ~~area~~ cell array to an output terminal only when a sum provided by the adder includes all 1s.

Claim 47 (Currently Amended): The data storage medium of claim 46, wherein

the first memory ~~area~~ cell array is read-only and stores first certification data that is unique to the data storage medium, and the second memory ~~area~~ cell array stores data and second certification data supplied from the outside; and

the data storage medium further comprises:

an encoder which encodes the first certification data into third certification data;

a specific memory area defined in the second memory ~~area~~ cell array according to the first certification data, to store the third certification data;

an identity circuit which determines whether or not the second and third certification data are identical with each other; and

a switch circuit which provides the data stored in the second memory ~~area~~ cell array to the outside only when the identity circuit determines that the second and third certification data are identical with each other.

Claim 48 (Currently Amended): The data storage medium of claim 47, wherein the first and second memory ~~areas~~ cell arrays are reserved in a NAND-type flash memory.

Claim 49 (Currently Amended): The data storage medium of claim 47, wherein the identity circuit comprises:

a generator which generates inverted binary data from binary data corresponding to the third certification data; and

an adder which adds the inverted binary data of the third certification data to binary data corresponding to the second certification data, and wherein the switch circuit comprises:

a circuit which connects the second memory ~~area~~ cell array to an output terminal only when a sum provided by the adder includes all 1s.

Claim 50 (Previously Presented): The data storage medium of claim 47, wherein the specific memory area stores binary data and inverted binary data both corresponding to the third certification data.

Claim 51 (Previously Presented): The data storage medium of claim 47, further comprising:

a tester which tests to see if the third certification data was altered; and

another switch circuit which provides the third certification data to the outside only when the tester determines that the first certification data was not altered.

Claim 52 (Previously Presented): The data storage medium of claim 51, wherein the tester comprises:

a reader which reads the binary data and inverted binary data both corresponding to the third certification data from the specific memory area; and

an adder which adds the read binary data and inverted binary data to each other, and wherein the switch circuit comprises:

a circuit which connects the specific memory area to an output terminal only when a sum provided by adder includes all 1s.